GIGALOG

56Gbps 8bit ADC

Gigalog Project Example

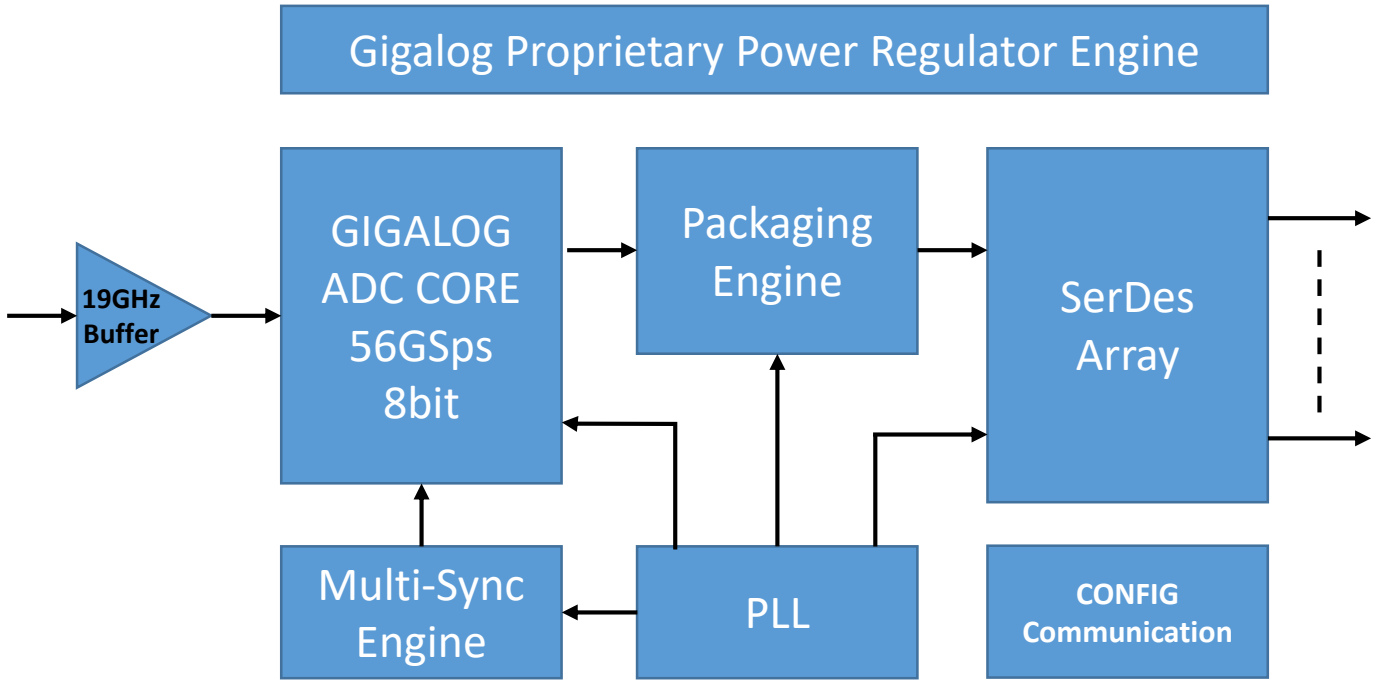
This document contains one of Gigalog projects that was supplied to the final customer. All information in this document provided with customer approval.

For any inquiries, please contact info@gigalogchip.com

Customer Requirements

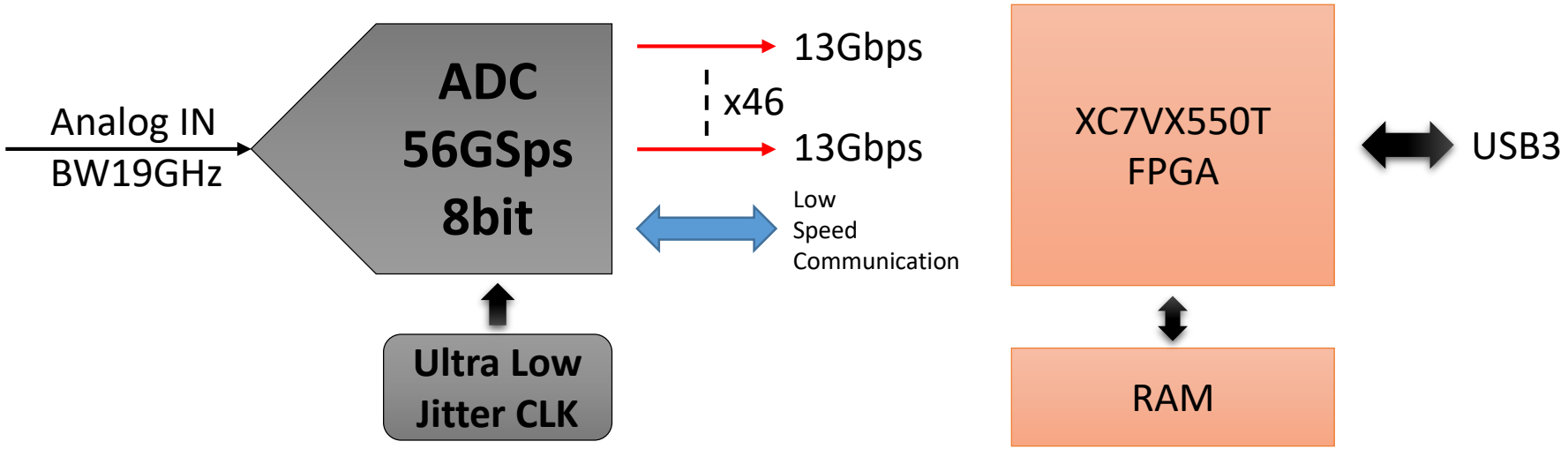
- Design ADC ASIC
  - 56GSps
  - 8bit
  - 6 enob
  - Ultralow Padc (~0.5W)
- Design Tester Board for ADC verification
- Use CMOS TSMC 28nm

IC Block Diagram



- IC, based on 28nm foundry.
- 56GSps – 46 SerDeses of up to 13.1Gbps
- Gigalog Proprietary ADC architecture, PLL, Gigalog 13Gbps SerDes, Special Equalization IO

Block Diagram



- PCB Based on Multilayer Ceramic LTCC Board
- Ultra low jitter oscillator is used (special cooled oscillator)
- Data is samples, sent to FPGA, processed and result sent to PC (Special mode of buffered RAM acquisition is implemented)

Summary

- Gigalog has proven experience of providing world fastest data converters.
- Huge Experience with ultralow Noise ASIC designs. World leaders in low noise, fast speed, analog IC design.